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SiC Technology

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6.1 Introduction

Silicon carbide (SiC)-based semiconductor electronic devices and circuits are presently being developed for use in high-temperature, high-power, and/or high-radiation conditions under which conventional semiconductors cannot adequately perform. Silicon carbide's ability to function under such extreme conditions is expected to enable significant improvements to a far-ranging variety of applications and systems. These range from greatly improved high-voltage switching[1–4] for energy savings in public electric power distribution and electric motor drives, to more powerful microwave electronics for radar and communications,[5–7] to sensors and controls for cleaner-burning more fuel-efficient jet aircraft and automobile engines. In the particular area of power devices, theoretical appraisals have indicated that SiC power MOSFETs and diode rectifiers would operate over higher voltage and temperature ranges, have superior switching characteristics, and yet have die sizes nearly 20 times smaller than correspondingly rated silicon-based devices.[8] However, these tremendous theoretical advantages have yet to be realized in experimental SiC devices, primarily due to the fact that SiC's relatively immature crystal growth and device fabrication technologies are not yet sufficiently developed to the degree required for reliable incorporation into most electronic systems.[9]

This chapter briefly surveys the SiC semiconductor electronics technology. In particular, the differences (both good and bad) between SiC electronics technology and well-known silicon VLSI technology are highlighted. Projected performance benefits of SiC electronics are highlighted for several large-scale applications. Key crystal growth and device-fabrication issues that presently limit the performance and capability of high-temperature and/or high-power SiC electronics are identified.

6.2 Fundamental SiC Material Properties

SiC Crystallography: Important Polytypes and Definitions

Silicon carbide occurs in many different crystal structures, called polytypes. A comprehensive introduction to SiC crystallography and polytypism can be found in Ref. 10. Despite the fact that all SiC polytypes chemically consist of 50% carbon atoms covalently bonded with 50% silicon atoms, each SiC polytype has its own distinct set of electrical semiconductor properties. While there are over 100 known polytypes of SiC, only a few are commonly grown in a reproducible form acceptable for use as an electronic semiconductor. The most common polytypes of SiC presently being developed for electronics are 3C-SiC, 4H-SiC, and 6H-SiC. 3C-SiC, also referred to as β-SiC, is the only form of SiC with a cubic crystal lattice structure. The non-cubic polytypes of SiC are sometimes ambiguously referred to as α-SiC. 4H-SiC and 6H-SiC are only two of many possible SiC polytypes with hexagonal crystal structure. Similarly, 15R-SiC is the most common of many possible SiC polytypes with a rhombohedral crystal structure.

Because some important electrical device properties are non-isotropic with respect to crystal orientation, lattice site, and surface polarity, some further understanding of SiC crystal structure and terminology is necessary. As discussed much more thoroughly in Ref. 10, different polytypes of SiC are actually composed of different stacking sequences of Si-C bilayers (also called Si-C double layers), where each single Si-C bilayer can simplistically be viewed as a planar sheet of silicon atoms coupled with a planar sheet of carbon atoms. The plane formed by a bilayer sheet of Si and C atoms is known as the basal plane, while the crystallographic *c*-axis direction, also known as the stacking direction or the [0001] direction, is defined normal to Si-C bilayer plane. Figure 6.1 schematically depicts the stacking sequence of the 6H-SiC polytype, which requires six Si-C bilayers to define the unit cell repeat distance along the *c*-axis [0001] direction. The [1100] direction depicted in Fig. 6.1 is often referred to as the a-axis direction. The silicon atoms labeled "h" or "k" in Figure 6.1 denote Si-C double layers that reside in "quasi-hexagonal" or "quasi-cubic" environments with respect to their immediately neighboring above and below bilayers. SiC is a polar semiconductor across the *c*-axis, in that one surface normal to the *c*-axis is terminated with silicon atoms, while the opposite normal *c*-axis surface is terminated with carbon atoms. As shown in Fig. 6.1, these surfaces are typically referred to as "silicon face" and "carbon face" surfaces, respectively.

SiC Semiconductor Electrical Properties

Owing to the differing arrangements of Si and C atoms within the SiC crystal lattice, each SiC polytype exhibits unique fundamental electrical and optical properties. Some of the more important semiconductor electrical properties of the 3C, 4H, and 6H silicon carbide polytypes are given in Table 6.1. Much more detailed electrical properties can be found in Refs. 11 to 13 and references therein. Even within a given polytype, some important electrical properties are non-isotropic, in that they are a strong function of crystallographic direction of current flow and applied electric field (e.g., electron mobility for 6H-SiC). Dopants in SiC can incorporate into energetically inequivalent quasi-hexagonal (*h*) C-sites or Si-sites, or quasi-cubic (*k*) C-sites or Si-sites (only Si-sites are *h* or *k* labeled in Fig. 6.1). While all dopant ionization energies associated with various dopant incorporation sites should normally be considered for utmost accuracy, Table 6.1 lists only the shallowest ionization energies of each impurity.

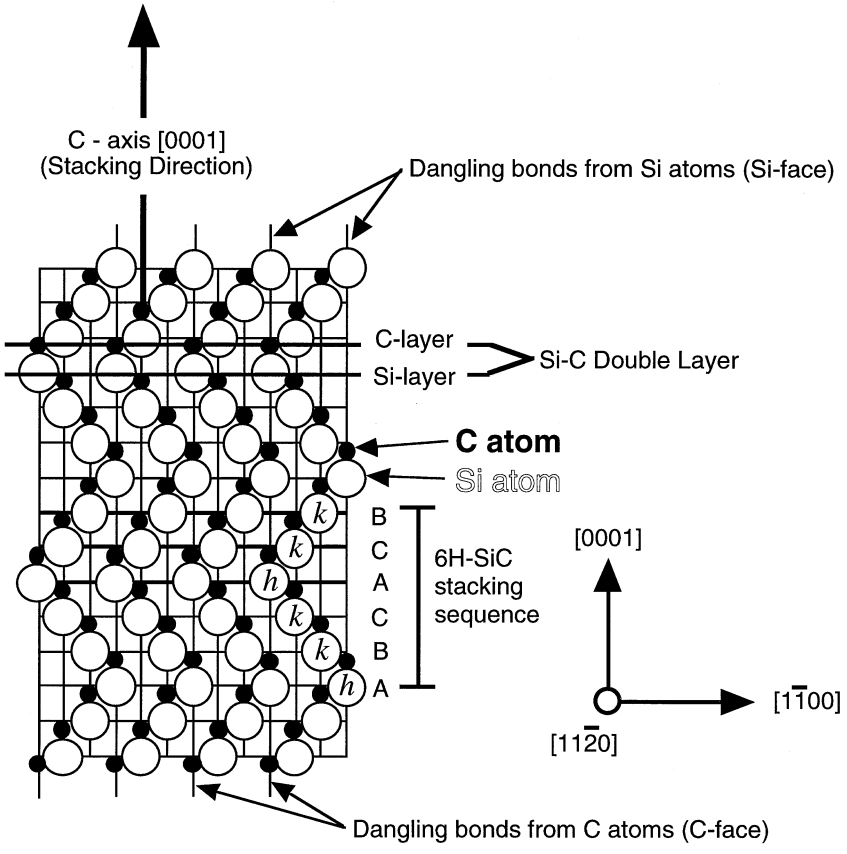

FIGURE 6.1 Schematic cross-section {(1120) plane} of the 6H-SiC polytype. (Modified from Ref. 10. With permission.)

TABLE 6.1 Comparison of Selected Important Semiconductors of Major SiC Polytypes with Silicon and GaAs

Property	Silicon	GaAs	4H-SiC	6H-SiC	3C-SiC
Bandgap (eV)	1.1	1.42	3.2	3.0	2.3
Relative dielectric constant	11.9	13.1	9.7	9.7	9.7
Breakdown field $N_D = 10^{17}$ cm^{-3} (MV/cm)	0.6	0.6	//*c*-axis: 3.0	// *c*-axis: 3.2 $\perp$ *c*-axis: >1	>1.5
Thermal conductivity (W/cm-K)	1.5	0.5	3–5	3–5	3–5
Intrinsic carrier concentration (cm^{-3})	10^{10}	1.8×10^6	~10^{-7}	~10^{-5}	~10
Electron mobility @ $N_D = 10^{16}$ cm^{-3} (cm^2/V-s)	1200	6500	//*c*-axis: 800 $\perp$ *c*-axis: 800	//*c*-axis: 60 $\perp$ *c*-axis: 400	750
Hole mobility @ $N_A = 10^{16}$ cm^{-3} (cm^2/V-s)	420	320	115	90	40
Saturated electron velocity (10^7 cm/s)	1.0	1.2	2	2	2.5
Donor dopants & shallowest ionization energy (meV)	P: 45 As: 54	Si: 5.8	N: 45 P: 80	N: 85 P: 80	N: 50
Acceptor dopants & shallowest ionization energy (meV)	B: 45	Be, Mg, C: 28	Al: 200 B: 300	Al: 200 B: 300	Al: 270
1998 Commercial wafer diameter (cm)	30	15	5	5	None

Note: Data compiled from Refs. 11–13, 15, and references therein. (With permission.)

For comparison, Table 6.1 also includes comparable properties of silicon and GaAs. Because silicon is the semiconductor employed in most commercial solid-state electronics, it is the yardstick against which other semiconductor materials must be evaluated. To varying degrees, the major SiC polytypes exhibit advantages and disadvantages in basic material properties compared to silicon. The most beneficial inherent material superiorities of SiC over silicon listed in Table 6.1 are its exceptionally high breakdown electric field, wide bandgap energy, high thermal conductivity, and high carrier saturation velocity. The electrical device performance benefits that each of these properties enable are discussed in the next section, as are system-level benefits enabled by improved SiC devices.

6.3 Applications and Benefits of SiC Electronics

Two of the most beneficial advantages that SiC-based electronics offer are in the areas of high-temperature device operation and high-power device operation. The specific SiC device physics that enables high-temperature and high-power capabilities will be examined first, followed by several examples of revolutionary system-level performance improvements these enhanced capabilities enable.

High-Temperature Device Operation

The wide bandgap energy and low intrinsic carrier concentration of SiC allow SiC to maintain semiconductor behavior at much higher temperatures than silicon, which in turn permits SiC semiconductor device functionality at much higher temperatures than silicon. As discussed in basic semiconductor physics textbooks,[14,15] semiconductor electronic devices function in the temperature range where intrinsic carriers are negligible so that conductivity is controlled by intentionally introduced dopant impurities. Furthermore, the intrinsic carrier concentration n_i is a fundamental prefactor to well-known equations governing undesired junction reverse-bias leakage currents.[15–18] As temperature increases, intrinsic carriers increase exponentially so that undesired leakage currents grow unacceptably large, and eventually at still higher temperatures, the semiconductor device operation is overcome by uncontrolled conductivity as intrinsic carriers exceed intentional device dopings. Depending on specific device design, the intrinsic carrier concentration of silicon generally confines silicon device operation to junction temperatures less than 300°C. The much smaller intrinsic carrier concentration of SiC theoretically permits device operation at junction temperatures exceeding 800°C; 600°C SiC device operation has been experimentally demonstrated on a variety of SiC devices (Section 6.6).

High-Power Device Operation

The high breakdown field and high thermal conductivity of SiC, coupled with high operational junction temperatures, theoretically permit extremely high-power densities and efficiencies to be realized in SiC devices. Figures 6.2 and 6.3 demonstrate the theoretical advantage of SiC's high breakdown field compared to silicon in shrinking the drift-region and associated parasitic on-state resistance of a 3000 V rated unipolar power MOSFET device.[8] The high breakdown field of SiC relative to silicon enables the blocking voltage region to be roughly 10X thinner and 10X heavier-doped, permitting a roughly 100-fold decrease in the dominant blocking region (N-Drift Region) resistance R_D of Fig. 6.2 for the SiC device relative to an identically rated 3000-V silicon power MOSFET.

Significant energy losses in many silicon high-power system circuits, particularly hard-switching motor drive and power conversion circuits, arise from semiconductor switching energy loss.[1,19] While the physics of semiconductor device switching loss are discussed in detail elsewhere,[15–17] switching energy loss is often a function of the turn-off time of the semiconductor switching device, generally defined as the time lapse between when a turn-off bias is applied and the time that the device actually cuts off most current flow. The faster a device turns off, the smaller its energy loss in a switched power conversion circuit. For device-topology reasons discussed in Refs. 8, 20–22, SiC's high breakdown field and wide energy bandgap enable much faster power switching than is possible in comparably volt-amp rated silicon power-switching devices. Therefore, SiC-based power converters could operate at higher switching

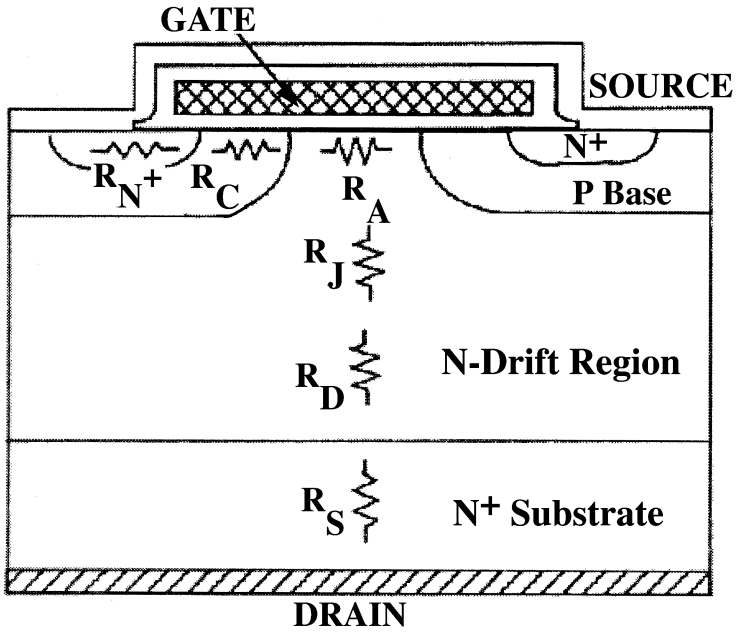

FIGURE 6.2 Cross-section of power MOSFET structure showing various internal resistances. The resistance R_D of the N-Drift Region is the dominant resistance in high-voltage power devices. (From Ref. 8. With permission.)

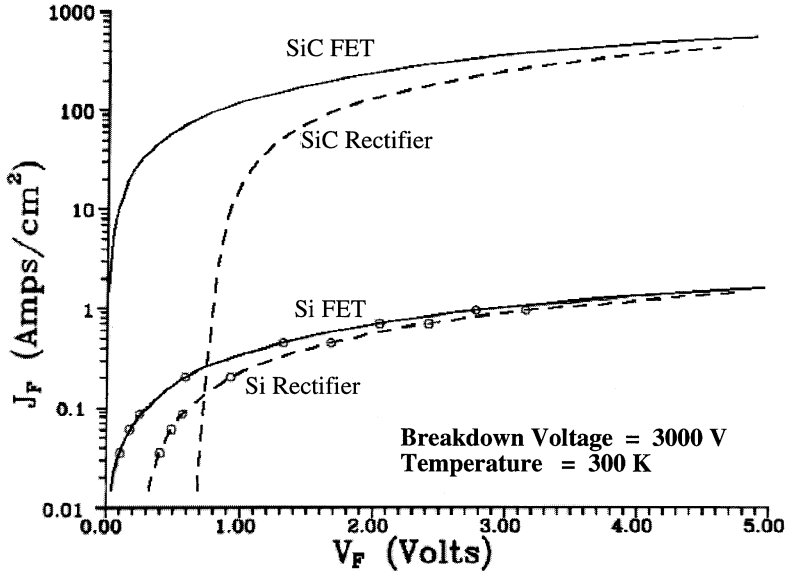

FIGURE 6.3 Simulated forward conduction characteristics of ideal Si and SiC 3000 V power MOSFETs and Schottky rectifiers. The high breakdown field of SiC relative to silicon (Table 6.1) enables the blocking voltage region (N-Drift Region in Fig. 6.2) to be roughly 10X thinner and 10X heavier-doped, permitting a roughly 100-fold increase in on-state current density for the 3000-V SiC devices relative to 3000-V silicon devices. (From Ref. 8. With permission.)

frequencies with much greater efficiency (i.e., less switching energy loss). Higher switching frequency in power converters is highly desirable because it permits use of proportionally smaller capacitors, inductors, and transformers, which in turn can greatly reduce overall system size and weight.

While SiC's smaller on-resistance and faster switching help minimize energy loss and heat generation, SiC's higher thermal conductivity enables more efficient removal of waste heat energy from the active device. Because heat energy radiation efficiency increases greatly with increasing temperature difference between the device and the cooling ambient, SiC's ability to operate at high junction temperatures permits much more efficient cooling to take place, so that heatsinks and other device-cooling hardware (i.e., fan cooling, liquid cooling, air conditioning, etc.) typically needed to keep high-power devices from overheating can be made much smaller or even eliminated.

While the preceding discussion focused on high-power switching for power conversion, many of the same arguments can be applied to devices used to generate and amplify RF signals used in radar and communications applications. In particular, the high breakdown voltage and high thermal conductivity, coupled with high carrier saturation velocity, allow SiC microwave devices to handle much higher power densities than their silicon or GaAs RF counterparts, despite SiC's disadvantage in low-field carrier mobility (Section 6.6).[6,7,23]

System Benefits of High-Power, High-Temperature SiC Devices

Uncooled operation of high-temperature and/or high-power SiC electronics would enable revolutionary improvements to aerospace systems. Replacement of hydraulic controls and auxiliary power units with distributed "smart" electromechanical controls capable of harsh-ambient operation will enable substantial jet-aircraft weight savings, reduced maintenance, reduced pollution, higher fuel efficiency, and increased operational reliability.[24–26] SiC high-power solid-state switches will also enable large efficiency gains in electric power management and control. Performance gains from SiC electronics could enable the public power grid to provide increased consumer electricity demand without building additional generation plants, and improve power quality and operational reliability through "smart" power management. More efficient electric motor drives will benefit industrial production systems as well as transportation systems such as diesel-electric railroad locomotives, electric mass-transit systems, nuclear-powered ships, and electric automobiles and buses.

From the above discussions, it should be apparent that SiC high-power and/or high-temperature solid-state electronics promise tremendous advantages that could significantly impact transportation systems and power usage on a global scale. By improving the way in which electricity is distributed and used, improving electric vehicles so that they become more viable replacements for internal combustion-engine vehicles, and improving the fuel efficiency and reducing pollution of remaining fuel-burning engines and generation plants, SiC electronics promises the potential to better the daily lives of all citizens of planet Earth.

6.4 SiC Semiconductor Crystal Growth

As of this writing, much of the outstanding theoretical promise of SiC electronics highlighted in the previous section has largely gone unrealized. A brief historical examination quickly shows that serious shortcomings in SiC semiconductor material manufacturability and quality have greatly hindered the development of SiC semiconductor electronics. From a simple-minded point of view, SiC electronics development has very much followed the general rule of thumb that a solid-state electronic device can only be as good as the semiconductor material from which it is made.

Historical Lack of SiC Wafers

Most of silicon carbide's superior intrinsic electrical properties have been known for decades. At the genesis of the semiconductor electronics era, SiC was considered an early transistor material candidate, along with germanium and silicon. However, reproducible wafers of reasonable consistency, size, quality,

and availability are a prerequisite for commercial mass-production of semiconductor electronics. Many semiconductor materials can be melted and reproducibly recrystallized into large, single crystals with the aid of a seed crystal, such as in the Czochralski method employed in the manufacture of almost all silicon wafers, enabling reasonably large wafers to be mass-produced. However, because SiC sublimes instead of melting at reasonably attainable pressures, SiC cannot be grown by conventional melt-growth techniques. This prevented the realization of SiC crystals suitable for mass-production until the late 1980s. Prior to 1980, experimental SiC electronic devices were confined to small (typically ~1 cm^2), irregularly shaped SiC crystal platelets (Fig. 6.4, right side) grown as a by-product of the Acheson process for manufacturing industrial abrasives (e.g., sandpaper)[27] or by the Lely process.[28] In the Lely process, SiC sublimed from polycrystalline SiC powder at temperatures near 2500°C are randomly condensed on the walls of a cavity forming small hexagonally shaped platelets. While these small, nonreproducible crystals permitted some basic SiC electronics research, they were clearly not suitable for semiconductor mass-production. As such, silicon became the dominant semiconductor fueling the solid-state technology revolution, while interest in SiC-based microelectronics was limited.

Growth of 3C-SiC on Large-Area (Silicon) Substrates

Despite the absence of SiC substrates, the potential benefits of SiC hostile-environment electronics nevertheless drove modest research efforts aimed at obtaining SiC in a manufacturable wafer form. Toward this end, the heteroepitaxial growth of single-crystal SiC layers on top of large-area silicon substrates was first carried out in 1983,[29] and subsequently followed by a great many others over the years using a variety of growth techniques. Primarily due to large differences in lattice constant (20% difference between SiC and Si) and thermal expansion coefficient (8% difference), heteroepitaxy of SiC using silicon as a substrate always results in growth of 3C-SiC with a very high density of crystallographic structural defects such as stacking faults, microtwins, and inversion domain boundaries.[30,31] Furthermore, the as-grown surface morphology of 3C-SiC grown on silicon is microscopically textured, making submicron lithography somewhat problematic. Other large-area wafer materials, such as sapphire, silicon-on-insulator, TiC, etc., have been employed as substrates for heteroepitaxial growth of SiC epilayers, but the resulting films have been of comparably poor quality with high crystallographic defect densities.

While some limited semiconductor electronic devices and circuits have been implemented in 3C-SiC grown on silicon,[32,33] the performance of these electronics can be summarized as severely limited by the high density of crystallographic defects to the degree that almost none of the operational benefits discussed in Section 6.3 have been viably realized. Among other problems, the crystal defects "leak" parasitic current across reverse-biased device junctions where current flow is not desired. Because excessive crystal defects lead to electrical device shortcomings, there are as yet no commercial electronics manufactured in 3C-SiC grown on large-area substrates.

Despite the lack of major technical progress, there is strong economic motivation to continue to pursue heteroepitaxial growth of SiC on large-area substrates, as this would provide cheap wafers for SiC electronics that would be immediately compatible with silicon integrated circuit manufacturing equipment. If ongoing work ever solves the extremely challenging crystallographic defect problems associated with the heteroepitaxial growth of SiC, it would likely become the material of choice for mass-production of SiC-based electronics. Given the present electrical deficiencies of heteroepitaxial SiC, 3C-SiC grown on silicon is more likely to be commercialized as a mechanical material in microelectromechanical systems (MEMS) applications (Section 6.6) instead of being used purely as a semiconductor in traditional solid-state electronics.

Sublimation Growth of SiC Wafers

In the late 1970s, Tairov and Tzvetkov established the basic principles of a modified seeded sublimation growth process for growth of 6H-SiC.[34,35] This process, also referred to as the modified Lely process, was a breakthrough for SiC in that it offered the first possibility of reproducibly growing acceptably large

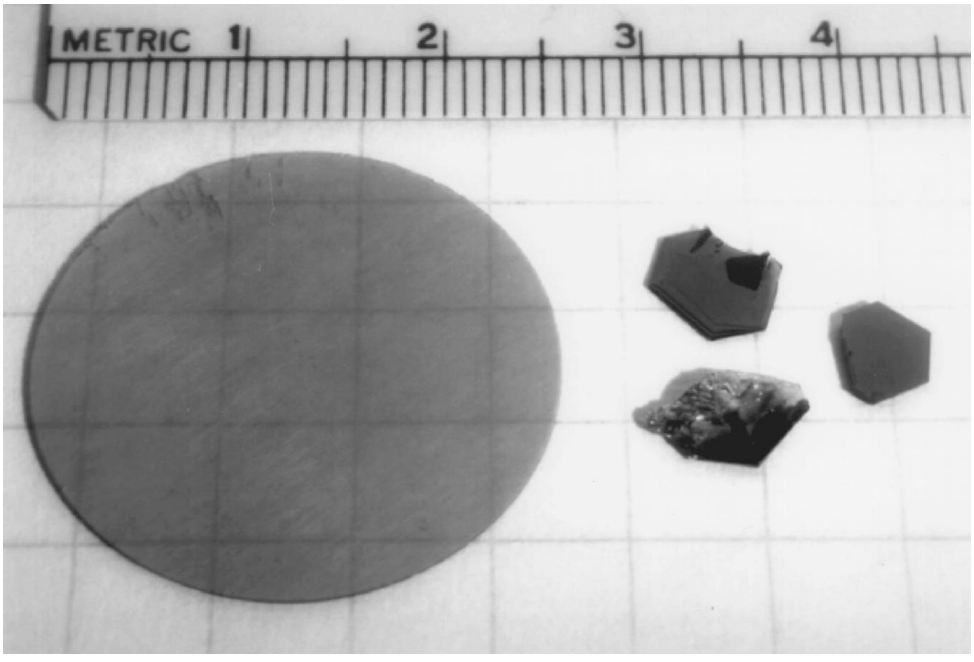

FIGURE 6.4 Mass-produced 2.5-cm diameter 6H-SiC wafer manufactured circa 1990 via seeded sublimation by Cree Research (left), and 6H-SiC Lely and Acheson platelet crystals (right) representative of single-crystal SiC substrates available prior to 1989. 5.1-cm diameter seeded sublimation SiC wafers entered the commercial market in 1997.

single crystals of SiC that could be cut and polished into mass-produced SiC wafers. The basic growth process is based on heating polycrystalline SiC source material to ~2400°C under conditions where it sublimes into the vapor phase and subsequently condenses onto a cooler SiC seed crystal. This produces a somewhat cylindrical boule of single-crystal SiC that grows taller at a rate of a few millimeters per hour. To date, the preferred orientation of the growth in the sublimation process is such that vertical growth of a taller cylindrical boule proceeds along the [0001] crystallographic *c*-axis direction (i.e., vertical direction in Fig. 6.1). Circular "*c*-axis" wafers with surfaces that lie normal (perpendicular) to the *c*-axis can be sawed from the roughly cylindrical boule. While other growth orientations (such as growth along the a-axis) continue to be investigated, the electronic quality of this material has thus far proven inferior to *c*-axis-grown wafers.[36,37]

Commercially Available SiC Wafers

After years of further development of the sublimation growth process, Cree Research became the first company to sell 2.5-cm diameter semiconductor wafers of 6H-SiC (Fig. 6.4, left side) in 1989.[38] Only with the development of the modified Lely seeded sublimation growth technique have acceptably large and reproducible single-crystal SiC wafers of usable electrical quality become available. Correspondingly, the vast majority of silicon carbide semiconductor electronics development has taken place since 1990. Other companies have subsequently entered the SiC wafer market, and sublimation grown wafers of the 4H-SiC polytype have also been commercialized, as summarized in Table 6.2.

Commercially available 4H- and 6H-SiC wafer specifications are given in Table 6.2. N-type, p-type, and semi-insulating SiC wafers are commercially available at different prices. Wafer size, cost, and quality are all very critical to the manufacturability and process yield of mass-produced semiconductor microelectronics. Compared to commonplace silicon and GaAs wafer standards, present-day 4H- and 6H-SiC wafers are small, expensive, and generally of inferior quality. In addition to high densities of crystalline defects such as micropipes and closed-core screw dislocations discussed in the next subsection,

TABLE 6.2 Commercial Vendors and Specifications of Selected Sublimation-Grown SiC Single-Crystal Wafers

Vendor [Ref.]	Year	Product	Wafer Diameter	Micropipes (#/cm^2)	Price (U.S.$)
Cree	1993	6H n-type, Si-face, R-Grade	3.0 cm	200–1000	1000
[38]		6H n-type, Si-face, P-Grade	3.0 cm	200–1000	2900
		6H n-type, C-face, P-Grade	3.0 cm	200–1000	3000
		6H p-type, Si-face, P-Grade	3.0 cm	200–1000	3300
		4H n-type, Si-face, R-Grade	3.0 cm	200–1000	3800
Cree	1997	4H n-type, Si-face, R-Grade	3.5 cm	100–200	750
[38]		4H n-type, Si-face, P-Grade	3.5 cm	100–200	1300
		4H n-type, Si-face, P-Grade	3.5 cm	<30	2300
	1998	4H n-type, Si-face, R-Grade	5.1 cm	<200	2100
		4H n-type, Si-face, P-Grade	5.1 cm	<200	3100
	1997	4H p-type, Si-face, R-Grade	3.5 cm	<200	1900
		4H Semi-Insulating, R-Grade	3.5 cm	<200	4800
		6H n-type, Si-face, P-Grade	3.5 cm	<200	1000
		6H p-type, Si-face, P-Grade	3.5 cm	<200	2200
Nippon Steel [142]	1997	4H n-type	2.5 cm	NA	NA
SiCrystal [143]	1997	4H n-type, Quality I	3.5 cm	<200	1200
		4H n-type, Quality III	3.5 cm	400–1000	900
		4H n-type, Quality I	2.5 cm	<200	600
		6H n-type, Quality I	3.5 cm	<200	1200
Sterling and	1998	6H n-type	3.5 cm	<100	800
ATMI/Epitronics		4H n-type	3.5 cm	<100	800
[144][145]					

commercial SiC wafers also exhibit significantly rougher surfaces, and larger warpage and bow than is typical for silicon and GaAs wafers.[39] This disparity is not surprising considering that silicon and GaAs wafers have undergone several decades of commercial process refinement, and that SiC is an extraordinarily hard material, making it very difficult to properly saw and polish. Nevertheless, ongoing wafer sawing and polishing process improvements should eventually alleviate wafer surface quality deficiencies.

SiC Wafer Crystal Defects

While the specific electrical effects of SiC crystal defects are discussed later in Section 6.6, the micropipe defect (Table 6.2) is regarded as the most damaging defect that is limiting upscaling of SiC electronics capabilities.[9,40] A micropipe is a screw dislocation with a hollow core and a larger Burgers vector, which becomes a tubular void (with a hollow diameter on the order of micrometers) in the SiC wafer that extends roughly parallel to the crystallographic *c*-axis normal to the polished *c*-axis wafer surface.[41–44] Sublimation-grown 4H- and 6H-SiC wafers also contain high densities of closed-core screw dislocation defects that, like micropipes, cause a considerable amount of localized strain and SiC lattice deformation.[42,43,45,46] Similar to horizontal branches on a tree with its trunk running up the *c*-axis, dislocation loops emanate out along the basal plane from screw dislocations.[41,47] As shown in Table 6.2, micropipe densities in commercial SiC wafers have shown steady improvement over a 5-year period, leading to wafers with less than 30 micropipes per square centimeter of wafer area. However, as discussed in Section 6.6, SiC wafer improvement trends will have to accelerate if some of SiC's most beneficial high-power applications are going to reach timely commercial fruition.

SiC Epilayers

Most SiC electronic devices are not fabricated directly in sublimation-grown wafers, but are instead fabricated in much higher quality epitaxial SiC layers that are grown on top of the initial sublimation-grown wafer. Well-grown SiC epilayers have superior electrical properties and are more controllable and reproducible than bulk sublimation-grown SiC wafer material. Therefore, the controlled growth of high-quality epilayers is highly important in the realization of useful SiC electronics.

SiC Epitaxial Growth Processes

An interesting variety of SiC epitaxial growth methodologies — ranging from liquid-phase epitaxy, molecular beam epitaxy, and chemical vapor deposition — has been investigated.[11,12,32] The chemical vapor deposition (CVD) growth technique is generally accepted as the most promising method for attaining epilayer reproducibility, quality, and throughputs required for mass-production. In simplest terms, variations of SiC CVD are carried out by heating SiC substrates in a chamber with flowing silicon and carbon containing gases that decompose and deposit Si and C onto the wafer, allowing an epilayer to grow in a well-ordered single-crystal fashion under well-controlled conditions. Conventional SiC CVD epitaxial growth processes are carried out at substrate growth temperatures between 1400 and 1600°C at pressures from 0.1 to 1 atm, resulting in growth rates on the order of micrometers per hour.[39,48–50] Higher-temperature (up to 2000°C) SiC CVD growth processes are also being pioneered to obtain higher SiC epilayer growth rates — on the order of hundreds of micrometers per hour.[51]

SiC Homoepitaxial Growth

Homoepitaxial growth, whereby the polytype of the SiC epilayer matches the polytype of the SiC substrate, is accomplished by step-controlled epitaxy.[39,49,52] Step-controlled epitaxy is based on growing epilayers on an SiC wafer polished at an angle (called the "tilt-angle" or "off-axis angle") of typically 3° to 8° off the (0001) basal plane, resulting in a surface with atomic steps and flat terraces between steps, as schematically depicted in Fig. 6.5. When growth conditions are properly controlled and there is a sufficiently short distance between steps, Si and C atoms impinging onto the growth surface find their way to steps where they bond and incorporate into the crystal. Thus, ordered lateral "step flow" growth takes place, which enables the polytypic stacking sequence of the substrate to be exactly mirrored in the growing epilayer. When growth conditions are not properly controlled or when steps are too far apart (as can occur with SiC substrate surfaces that are polished to within less than 1° of the basal plane), growth adatoms can nucleate and bond in the middle of terraces instead of at the steps; this leads to heteroepitaxial growth of poor-quality 3C-SiC.[39,49] To help prevent spurious nucleation of 3C-SiC "triangular inclusions" during epitaxial growth, most commercial 4H- and 6H-SiC substrates are polished to tilt angles of 8° and 3.5° off the (0001) basal plane, respectively.

It is important to note that most present-day, as-grown SiC epilayers contain varying densities of undesirable surface morphological features that could affect SiC device processing and performance.[39,48] In addition to "triangular inclusions," these include "growth pits" as well as large macrosteps formed by coalescence of multiple SiC growth steps (i.e., "step bunching") during epitaxy. Pre-growth wafer polishing as well as growth initiation procedures have been shown to strongly impact the formation of undesirable epitaxial growth features.[39,48] Further optimization of pre-growth treatments and epitaxial growth initiation processes are expected to reduce undesired morphological growth features.

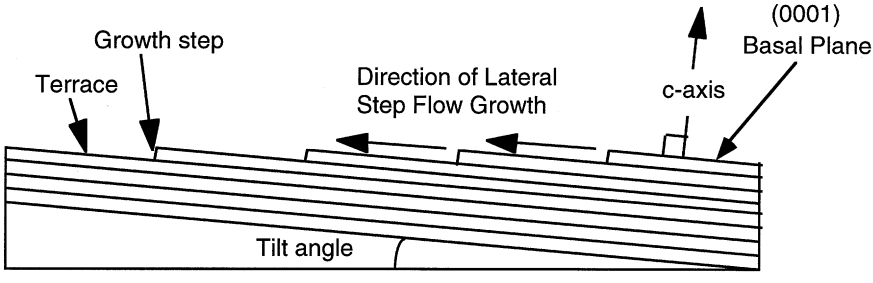

FIGURE 6.5 Cross-sectional schematic representation of "off-axis" polished SiC surface used for homoepitaxial growth. When growth conditions are properly controlled and there is a sufficiently short distance between steps, Si and C atoms impinging onto the growth surface find their way to steps where they bond and incorporate into the crystal. Thus, ordered lateral "step-flow" growth takes place, which enables the polytypic stacking sequence of the substrate to be exactly mirrored in the growing epilayer. (Modified from Ref. 10. With permission.)

SiC Epilayer Doping

In situ doping during CVD epitaxial growth is primarily accomplished through the introduction of nitrogen (usually N_2) for n-type and aluminum (usually trimethyl- or triethylaluminum) for p-type epilayers.[12] Some alternative dopants such as phosphorous, boron, and vanadium have also been investigated for n-type, p-type, and semi-insulating epilayers, respectively. While some variation in epilayer doping can be carried out strictly by varying the flow of dopant gasses, the site-competition doping methodology[53,54] has enabled a much broader range of SiC doping to be accomplished. In addition, site-competition epitaxy has also made moderate epilayer dopings more reliable and repeatable. The site-competition dopant-control technique is based on the fact that many dopants of SiC preferentially incorporate into either Si lattice sites or C lattice sites. As an example, nitrogen preferentially incorporates into lattice sites normally occupied by carbon atoms. By epitaxially growing SiC under carbon-rich conditions, most of the nitrogen present in the CVD system (whether it is a residual contaminant or intentionally introduced) can be excluded from incorporating into the growing SiC crystal. Conversely, by growing in a carbon-deficient environment, the incorporation of nitrogen can be enhanced to form very heavily doped epilayers for ohmic contacts. Aluminum, which is opposite to nitrogen, prefers the Si-site of SiC, and other dopants have also been controlled through site competition by properly varying the Si/C ratio during crystal growth. SiC epilayer dopings ranging from 9×10^{14} to 1×10^{19} cm^{-3} are commercially available, and researchers have reported obtaining dopings nearly a factor of 10 larger and smaller than this range for n-type and p-type dopings. Commercial epilayer thickness and doping tolerances are presently specified at 25% and 100%, respectively,[38] while doping uniformities of 7% and thickness uniformities of 4% over a 30-mm wafer have been reported in developmental research.[48]

SiC Epilayer Crystal Defects

Improvements in epilayer quality are needed as SiC electronics upscale toward production integrated circuits, as there are presently many observable defects present in state-of-the-art SiC homoepilayers. Non-ideal surface morphological features, such as "growth pits," 3C-SiC triangular inclusions ("triangle defects") introduced in Section 6.4, are generally more prevalent in 4H-SiC epilayers than 6H-SiC epilayers. Most of these features appear to be manifestations of non-optimal "step flow" during epilayer growth arising from substrate defects, non-ideal substrate surface finish, contamination, and/or unoptimized epitaxial growth conditions. While by no means trivial, it is anticipated that SiC epilayer surface morphology will greatly improve as refined substrate preparation and epilayer growth processes are developed.

Many impurities and crystallographic defects found in sublimation-grown SiC wafers do not propagate into SiC homoepitaxial layers. For example, basal-plane dislocation loops emanating from micropipes and screw dislocations in sublimation-grown SiC wafers (Section 6.4) are not generally observed in SiC epilayers.[47] Unfortunately, however, screw dislocations (both micropipes and closed-core screw dislocations) present in commercial *c*-axis wafers do replicate themselves up the crystallographic *c*-axis into SiC homoepilayers grown on commercial wafers. Therefore, as discussed later in Section 6.6, devices fabricated in commercial epilayers are still subject to electrical performance and yield limitations imposed by commercial substrate screw-dislocation defect densities.

Alternative Growth Methods to Reduce SiC Epilayer Dislocations

As of this writing, there is no known practical method of realizing screw-dislocation-free 4H- or 6H-SiC homoepilayers on conventional sublimation-grown substrates. Some non-conventional epitaxial growth techniques have been attempted in an effort to prevent the propagation of micropipes into an epilayer.[55,56] While these approaches have scored modest success in closing and covering up micropipes, to date there has been little, if any, improvement demonstrated in electrical devices fabricated in the resulting material. This is perhaps due to the fact that screw dislocations and associated harmful stresses may still be present in the epilayer, despite the fact that some open cores may have been converted to closed cores.

Because screw dislocations propagate up the *c*-axis, one could conceivably alleviate screw dislocations by growing epilayers on SiC wafers with their surface parallel to the *c*-axis using "a-axis" wafers. Unfortunately, efforts directed at realizing a-axis wafers and epilayers have to date been much less successful than *c*-axis wafers and epilayers, primarily because defects that form and propagate up the basal plane (the vertical wafer and epilayer growth direction in a-axis-oriented wafers) have proven more harmful and difficult to eliminate than screw dislocations in conventional *c*-axis wafers and epilayers.[36,37]

Selected-area epitaxial growth techniques have recently led to startling reductions in GaN epilayer defect densities.[57] While selective-area epitaxial growth of 3C-SiC has been demonstrated, the applicability of similar techniques to realizing superior electrical-quality SiC will be much more difficult due to the step-flow homoepitaxial growth mechanism of α-SiC as well as high growth temperatures (>1400°C), which are incompatible with conventional growth-masking materials like SiO_2.

6.5 SiC Device Fundamentals

In order to minimize the development and production costs of SiC electronics, it is essential that SiC device fabrication take advantage of the existing silicon and GaAs wafer processing infrastructure as much as possible. As will be discussed in this section, most of the steps necessary to fabricate SiC electronics starting from SiC wafers can be accomplished using somewhat modified commercial silicon electronics processes and fabrication tools.

Choice of Polytype for Devices

As discussed in Section 6.4, 4H-SiC and 6H-SiC are the far superior forms of semiconductor device quality SiC commercially available in mass-produced wafer form. Therefore, only 4H-SiC and 6H-SiC device processing methods will be explicitly considered in the rest of this section. It should be noted, however, that most of the processing methods discussed in this section are applicable to other polytypes of SiC, except for the case of 3C-SiC grown on silicon where all processing temperatures need to be kept well below the melting temperature of silicon (~1400°C).

It is generally accepted that 4H-SiC's substantially higher carrier mobility and shallower dopant ionization energies compared to 6H-SiC (Table 6.1) should make it the polytype of choice for most SiC electronic devices, provided that all other device processing, performance, and cost-related issues play out as being roughly equal between the two polytypes. Furthermore, the inherent mobility anisotropy that degrades conduction parallel to the crystallographic *c*-axis in 6H-SiC[58] will particularly favor 4H-SiC for vertical power device configurations (Section 6.6).

SiC Selective Doping: Ion Implantation

The fact that diffusion coefficients of most SiC dopants are negligibly small below ~1800°C is excellent for maintaining device junction stability, because dopants do not undesirably diffuse as the device is operated long-term at high-temperatures. Unfortunately, however, this characteristic also precludes the use of conventional dopant diffusion, a highly useful technique widely employed in silicon microelectronics manufacturing for patterned doping of SiC.

Laterally patterned doping of SiC is carried out by ion implantation. This somewhat restricts the depth to which most dopants can be conventionally implanted to less than 1 μm using conventional dopants and implantation equipment. Compared to silicon processes, SiC ion-implantation requires a much higher thermal budget to achieve acceptable dopant implant electrical activation. Summaries of ion-implantation processes for various dopants can be found in Refs. 11, 59, and 60. Most of these processes are based on carrying out implantation at elevated temperatures (~500 to 800°C) using a patterned high-temperature masking material. The elevated temperature during implantation promotes some lattice self-healing during the implant, so that damage and segregation of displaced silicon and carbon atoms does not become excessive, especially in high-dose implants often employed for ohmic

contact formation.[59,60] Co-implantation of carbon with p-type dopants has recently been investigated as a means to improve the electrical conductivity of implanted p-type contact layers.[61]

Following implantation, the patterning mask is stripped and a much higher temperature (~1200 to 1800°C) anneal is carried out to achieve maximum electrical activation of dopant donor or acceptor ions. The final annealing conditions are crucial for obtaining desired electrical properties from ion-implanted layers. At higher implant anneal temperatures, the SiC surface morphology can seriously degrade as damage-assisted sublimation etching of the SiC surface begins to take place.[62] Because sublimation etching is driven primarily by loss of silicon from the crystal surface, annealing in silicon overpressures can be used to prevent surface degradation during high-temperature anneals. Such overpressure can be achieved by close-proximity solid sources, such as using an enclosed SiC crucible with SiC lid and/or SiC powder near the wafer, or by annealing in a silane-containing atmosphere.

SiC Contacts and Interconnects

All useful semiconductor electronics require conductive signal paths in and out of each device, as well as conductive interconnects to carry signals between devices on the same chip and to external circuit elements that reside off-chip. While SiC itself is theoretically capable of fantastic operation under extreme conditions (Section 6.3), such functionality is useless without contacts and interconnects that are also capable of operation under the same conditions to enable complete extreme-condition circuit functionality. Previously developed conventional contact and interconnect technologies will likely not be sufficient for reliable operation in extreme conditions that SiC enables. The durability and reliability of metal–semiconductor contacts and interconnects are two of the main factors limiting the operational high-temperature limits of SiC electronics. Similarly, SiC high-power device contacts and metallizations will have to withstand both high-temperature and high current density stress never before encountered in silicon power electronics experience.

The subject of metal–semiconductor contact formation is a very important technical field, too broad to be discussed in detail here. For general background discussions on metal–semiconductor contact physics and formation, the reader should consult narratives presented in Refs. 15 and 63. These references primarily discuss ohmic contacts to conventional narrow-bandgap semiconductors such as silicon and GaAs. Specific overviews of SiC metal–semiconductor contact technology can be found in Refs. 64 to 67.

As discussed in Refs. 64 to 67, there are both similarities and a few differences between SiC ohmic contacts and ohmic contacts to conventional narrow-bandgap semiconductors (e.g., silicon, GaAs). The same basic physics and current transport mechanisms that are present in narrow-bandgap contacts — such as surface states, Fermi-pinning, thermionic emission, and tunneling — also apply to SiC contacts. A natural consequence of the wider bandgap of SiC is higher effective Schottky barrier heights. Analogous with narrow-bandgap ohmic contact physics, the microstructural and chemical state of the SiC–metal interface is crucial to contact electrical properties. Therefore, pre-metal-deposition surface preparation, metal deposition process, choice of metal, and post-deposition annealing can all greatly impact the resulting performance of metal–SiC contacts. Because the chemical nature of the starting SiC surface is strongly dependent on surface polarity, it is not uncommon to obtain significantly different results when the same contact process is applied to the silicon face surface vs. the carbon face surface.

SiC Ohmic Contacts

Ohmic contacts serve the purpose of carrying electrical current into and out of the semiconductor, ideally with no parasitic resistance. The properties of various ohmic contacts to SiC reported to date are summarized in Refs. 66 and 67. While SiC specific ohmic contact resistances at room temperature are generally higher than in contacts to narrow-bandgap semiconductors, they are nevertheless sufficiently low for most envisioned SiC applications. Lower specific contact resistances are usually obtained to n-type 4H- and 6H-SiC (~10^{-4} to 10^{-6} ohm-cm^2) than to p-type 4H- and 6H-SiC (~10^{-3} to 10^{-5} ohm-cm^2). Consistent with narrow-bandgap ohmic contact technology, it is easier to make low-resistance ohmic contacts to heavily doped SiC. While it is possible to achieve ohmic contacts to lighter-doped SiC using high-

temperature annealing, the lowest-resistance ohmic contacts are most easily implemented on SiC degenerately doped by site competition (Section 6.4) or high-dose ion implantation (Section 6.5). If the SiC doping is sufficiently degenerate, many metals deposited on a relatively clean SiC surface are ohmic in the "as deposited" state.[68] Regardless of doping, it is common practice in SiC to thermally anneal contacts to obtain the minimum possible ohmic contact resistance. Most SiC ohmic contact anneals are performed at temperatures around 1000°C in non-oxidizing environments. Depending on the contact metallization employed, this anneal generally causes limited interfacial reactions (usually metal-carbide or metal-silicide formation) that broaden and/or roughen the metal–semiconductor interface, resulting in enhanced conductivity through the contact.

Truly enabling harsh-environment SiC electronics will require ohmic contacts that can reliably withstand prolonged harsh-environment operation. Most reported SiC ohmic metallizations appear sufficient for long-term device operation up to 300°C. SiC ohmic contacts that withstand heat soaking under no electrical bias at 500 to 600°C for hundreds or thousands of hours in non-oxidizing gas or vacuum environments have also been demonstrated. In air, however, there has only been demonstration to date of a contact that can withstand heat soaking (no electrical bias) for 60 hours at 650°C.[69] Some very beneficial aerospace systems will require simultaneous high-temperature ($T > 300$°C) and high current density operation in oxidizing air environments. Electromigration, oxidation, and other electrochemical reactions driven by high-temperature electrical bias in a reactive oxidizing environment are likely to limit SiC ohmic contact reliability for the most demanding applications. The durability and reliability of SiC ohmic contacts is one of the critical factors limiting the practical high-temperature limits of SiC electronics.

SiC Schottky Contacts

Rectifying metal–semiconductor Schottky barrier contacts to SiC is useful for a number of devices, including metal–semiconductor field-effect transistors (MESFETs) and fast-switching rectifiers. References 64, 65, 67, and 70 summarize electrical results obtained in a variety of SiC Schottky studies to date. Due to the wide bandgap of SiC, almost all unannealed metal contacts to lightly doped 4H- and 6H-SiC are rectifying. Rectifying contacts permit extraction of Schottky barrier heights and diode ideality factors by well-known current-voltage (I-V) and capacitance-voltage (C-V) electrical measurement techniques.[63] While these measurements show a general trend that Schottky junction barrier height does somewhat depend on metal–semiconductor workfunction difference, the dependence is weak enough to suggest that surface state charge also plays a significant role in determining the effective barrier height of SiC Schottky junctions. At least some experimental scatter exhibited for identical metals can be attributed to cleaning and metal deposition process differences, as well as different barrier height measurement procedures. The work by Teraji et al.,[71] in which two different surface cleaning procedures prior to titanium deposition lead to ohmic behavior in one case and rectifying behavior in the other, clearly shows the important role that process recipe can play in determining SiC Schottky contact electrical properties.

It is worth noting that barrier heights calculated from C-V data are often somewhat higher than barrier heights extracted from I-V data taken from the same diode. Furthermore, the reverse current drawn in experimental SiC diodes, while small, is nevertheless larger than expected based on theoretical substitution of SiC parameters into well-known Schottky diode reverse leakage current equations developed for narrow-bandgap semiconductors. Bhatnagar et al.[72] proposed a model to explain these behaviors, in which localized surface defects, perhaps elementary screw dislocations where they intersect the SiC-metal interface, cause locally reduced junction barriers in the immediate vicinity of defects. Because current is exponentially dependent on Schottky barrier height, this results in the majority of measured current flowing at local defect sites instead of evenly distributed over the entire Schottky diode area. In addition to local defects, electric field crowding along the edge of the SiC Schottky barrier can also lead to increased reverse-bias leakage current and reduced reverse breakdown voltage.[15,16,63] Schottky diode edge termination techniques to relieve electric field edge crowding and improve Schottky rectifier reverse properties are discussed later in Section 6.6. Quantum mechanical tunneling of carriers through the barrier may also account for some excess reverse leakage current in SiC Schottky diodes.[73]

The high-temperature operation of rectifying SiC Schottky diodes is primarily limited by reverse-bias thermionic leakage of carriers over the junction barrier. Depending on the specific application and the barrier height of the particular device, SiC Schottky diode reverse leakage currents generally grow to excessive levels at around 300 to 400°C. As with ohmic contacts, electrochemical interfacial reactions must also be considered for long-term Schottky diode operation at the highest temperatures.

Patterned Etching of SiC for Device Fabrication

At room temperature, no known wet chemical etches single-crystal SiC. Therefore, most patterned etching of SiC for electronic devices and circuits is accomplished using dry etching techniques. The reader should consult Ref. 74; it contains an excellent summary of dry SiC etching results obtained to date. The most commonly employed process involves reactive ion etching (RIE) of SiC in fluorinated plasmas. Sacrificial etch masks (often aluminum metal) are deposited and photolithographically patterned to protect desired areas from being etched. The SiC RIE process can be implemented using standard silicon RIE hardware, and typical 4H- and 6H-SiC RIE etch rates are on the order of hundreds of angstroms per minute. Well-optimized SiC RIE processes are typically highly anisotropic with little undercutting of the etch mask, leaving smooth surfaces. One of the keys to achieving smooth surfaces is preventing "micromasking," wherein masking material is slightly etched and randomly redeposited onto the sample, effectively masking very small areas on the sample that were intended for uniform etching. This can result in "grass"-like etch-residue features being formed in the unmasked regions, which is undesirable in most cases. In special cases, RIE etching under conditions promoting micromasking is useful in greatly roughening the SiC surface to reduce the contact resistance of subsequently deposited ohmic metallizations.

While RIE etch rates are sufficient for many electronic applications, much higher SiC etch rates are necessary to carve features on the order of tens to hundreds of micrometers deep that are needed to realize advanced sensors, microelectromechanical systems (MEMS), and some very high-voltage power device structures. High-density plasma dry etching techniques, such as electron cyclotron resonance (ECR) and inductively coupled plasma (ICP), have been developed to meet the need for deep-etching of SiC. Residue-free patterned etch rates exceeding a thousand angstroms a minute have been demonstrated.[74–76]

Patterned etching of SiC at very high etch rates has also been demonstrated using photo-assisted and dark electrochemical wet etching.[77,78] By choosing proper etching conditions, this technique has demonstrated a very useful dopant-selective etch-stop capability. However, there are major incompatibilities of the electrochemical process that make it undesirable for VLSI mass-production, including extensive pre-etching and post-etching sample preparation, etch isotropy and mask undercutting, and somewhat non-uniform etching across the sample.

SiC Insulators: Thermal Oxides and MOS Technology

The vast majority of semiconductor integrated circuit chips in use today rely on silicon metal-oxide-semiconductor field effect transistors (MOSFETs), whose electronic advantages and operational device physics are summarized in Choma's chapter on devices and their models and elsewhere.[15,16,79] Given the extreme usefulness and success of MOSFET-based electronics in VLSI silicon, it is naturally desirable to implement high-performance inversion channel MOSFETs in SiC. Like silicon, SiC forms a thermal SiO_2 oxide when it is sufficiently heated in an oxygen environment. While this enables SiC MOS technology to somewhat follow the highly successful path of silicon MOS technology, there are nevertheless important differences in insulator quality and device processing that are presently preventing SiC MOSFETs from realizing their full beneficial potential. While the following discourse attempts to quickly highlight key issues facing SiC MOSFET development, more detailed insights can be found in Refs. 80 to 83. In highlighting the difficulties facing SiC MOSFET development, it is important to keep in mind that early silicon MOSFETs faced similar developmental challenges that took many years of dedicated research effort to successfully overcome.

From a purely electrical point of view, there are two prime operational deficiencies of SiC oxides and MOSFETs compared to silicon MOSFETs. First, effective inversion channel mobilities in most SiC MOSFETs are much lower (typically well under 100 cm^2/V-s for inversion electrons) than one would expect based on silicon inversion channel MOSFET carrier mobilities. This seriously reduces the transistor gain and current-carrying capability of SiC MOSFETs, so that SiC MOSFETs are not nearly as advantageous as theoretically predicted. Second, SiC oxides have not proven as reliable and immutable as well-developed silicon oxides, in that SiC MOSFETs are more prone to threshold voltage shifts, gate leakage, and oxide failures than comparably biased silicon MOSFETs. The excellent works by Cooper[80] and Brown et al.[83] discuss noteworthy differences between the basic electrical properties of n-type versus p-type SiC MOS devices. SiC MOSFET oxide electrical performance deficiencies appear mostly attributable to differences between silicon and SiC thermal oxide quality and interface structure that cause the SiC oxide to exhibit undesirably higher levels of interface state densities (~10^{11} to 10^{13} $eV^{-1}cm^{-2}$), fixed oxide charges (~10^{11} to 10^{12} cm^{-2}), charge trapping, carrier oxide tunneling, and roughness-related scattering of inversion channel carriers.

One of the most obvious differences between thermal oxidation of silicon and SiC to form SiO_2 is the presence of C in SiC. While most of the C in SiC converts to gaseous CO and CO_2 and escapes the oxide layer during thermal oxidation, leftover C species residing near the SiC–SiO_2 interface nevertheless appear to have a detrimental impact on SiO_2 electrical quality.[80,81] Cleaning treatments and oxidation/anneal recipes aimed at reducing interfacial C appear to improve SiC oxide quality. Another procedure employed to minimize detrimental carbon effects has been to form gate oxides by thermally oxidizing layers of silicon deposited on top of SiC.[84] Likewise, deposited insulators also show promise toward improving SiC MOSFET characteristics, as Sridevan et al.[85] have recently reported greatly improved SiC inversion channel carrier mobilities (>100 cm^2/V-s) using thick deposited gate insulators.

SiC surfaces are well known to be much rougher than silicon surfaces, due to off-angle polishing needed to support SiC homoepitaxy (Fig. 6.5) as well as step-bunching (particularly pronounced in 4H-SiC) that occurs during SiC homoepilayer growth (Section 6.4).[39,86] The impact of surface morphology on inversion channel mobility is highlighted by the recent work of Scharnholz et al.,[87] in which improved mobility (>100 cm^2/V-s) was obtained by specifically orienting SiC MOSFETs in a direction such that current flowed parallel to surface step texture. The interface roughness of SiC may also be a factor in poor oxide reliability by assisting unwanted injection of carriers that damage and degrade the oxide.

As Agarwal et al.[88] have pointed out, the wide bandgap of SiC reduces the potential barrier impeding tunneling of damaging carriers through SiC thermal oxides, so that perfectly grown oxides on atomically smooth SiC would not be as reliable as silicon thermal oxides. Therefore, it is highly probable that alternative gate insulators will have to be developed for optimized implementation of inversion-channel SiC FETs for the most demanding high-power and/or high-temperature electronic applications.

SiC Device Packaging and System Considerations

Hostile-environment SiC semiconductor devices and ICs are of little advantage if they cannot be reliably packaged and connected to form a complete system capable of hostile-environment operation. With proper materials selection, modifications of existing IC packaging technologies appear feasible for non-power SiC circuit packaging up to 300°C.[89,90] Prototype electronic packages that can withstand over a thousand hours of heat soaking without electrical bias at 500°C have been demonstrated.[91] Much work remains before electronics system packaging can meet the needs of the most demanding aerospace electronic applications, whose requirements include high-power operation in high-vibration, 500 to 600°C, oxidizing-ambient environments. Similarly, harsh-environment passive components, such as inductors, capacitors, and transformers, must also be developed for operation in demanding conditions before the full system-level benefits of SiC electronics discussed in Section 6.3 can be successfully realized.

6.6 SiC Electronic Devices and Circuits

This section briefly summarizes a variety of SiC electronic device designs broken down by major application areas. The operational performance of experimental SiC devices is compared to theoretically predicted SiC performance as well as the capabilities of existing silicon and GaAs devices. SiC process and materials technology issues limiting the capabilities of various SiC device topologies are highlighted as key issues to be addressed in further SiC technology maturation.

SiC Optoelectronic Devices

The wide bandgap of SiC is useful for realizing short wavelength blue and ultraviolet (UV) optoelectronics. 6H-SiC-based blue pn junction light-emitting diodes (LEDs) were the first silicon carbide-based devices to reach high-volume commercial sales. These epitaxially grown, dry-etch, mesa-isolated pn junction diodes were the first mass-produced LEDs to cover the blue (~250 to 280 nm peak wavelength) portion of the visible color spectrum, which in turn enabled the realization of the first viable full-color LED-based displays.[92] Because the SiC bandgap is indirect (i.e., the conduction minimum and valence band maximum do not coincide in crystal momentum space), luminescent recombination in the LEDs is governed by inherently inefficient indirect transitions mediated by impurities and phonons.[93] Therefore, the external quantum efficiency of SiC blue LEDs (i.e., percentage of light energy output obtained vs. electrical energy input) was limited to well below 1%. While commercially successful during the 1989 to 1995 timeframe, SiC-based blue LEDs have now been totally obsoleted by the emergence of much brighter, much more efficient, direct-bandgap GaN blue LEDs.

SiC has proven much more efficient at absorbing short-wavelength light, which has enabled the realization of SiC UV-sensitive photodiodes that serve as excellent flame sensors in turbine-engine combustion monitoring and control.[92,94] The wide bandgap of 6H-SiC is useful for realizing low photodiode dark currents, as well as sensors that are blind to undesired near-infrared wavelengths produced by heat and solar radiation. Commercial SiC-based UV flame sensors, again based on epitaxially grown, dry-etch, mesa-isolated 6H-SiC pn junction diodes, have successfully reduced harmful pollution emissions from gas-fired, ground-based turbines used in electrical power generation systems. Prototype SiC photodiodes are also being developed to improve combustion control in jet-aircraft engines.[95]

SiC RF Devices

The main use of SiC RF devices appears to lie in high-frequency solid-state high-power amplification at frequencies from around 600 MHz (UHF-band) to perhaps around 10 GHz (X-band). As discussed in better detail in Refs. 6, 7, 23, 96, and 97, the high breakdown voltage and high thermal conductivity, coupled with high carrier saturation velocity, allow SiC RF transistors to handle much higher power densities than their silicon or GaAs RF counterparts, despite SiC's disadvantage in low-field carrier mobility (Section 6.2). This power output advantage of SiC is briefly illustrated in Fig. 6.6 for the specific case of a Class A MESFET-based RF amplifier. The maximum theoretical RF power of a Class A MESFET operating along the DC load line shown in Fig. 6.6 is approximated by[7]:

$$P_{max} = \frac{I_{dson}(V_b - V_{knee})}{8} \tag{6.1}$$

The higher breakdown field of SiC permits higher drain breakdown voltage (V_b), permitting RF operation at higher drain biases. Given that there is little degradation in I_{dson} and V_{knee} for SiC vs. GaAs and silicon, the increased drain voltage directly leads to higher SiC MESFET output power densities. The higher thermal conductivity of SiC is also crucial in minimizing channel self-heating so that phonon scattering does not seriously degrade channel carrier velocity and I_{dson}. As discussed in Refs. 7 and 97, similar RF output power arguments can be made for SiC-based static induction transistors (SITs).

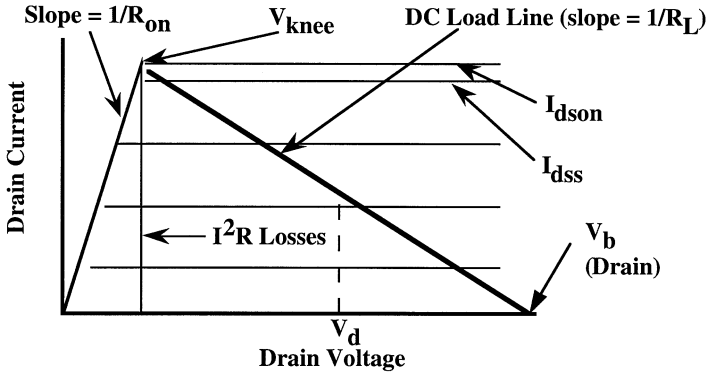

FIGURE 6.6 Piecewise linear MESFET drain characteristic showing DC load line used in Class A RF amplifier operation. The higher breakdown voltage V_b enabled by SiC's higher breakdown field enables operation at higher drain biases, leading to higher RF power densities. (From Ref. 7. With permission.)

The high power density of high-frequency SiC transistors could prove very useful in realizing solid-state transmitters for cell phone base stations, high-definition television (HDTV) transmitters, and radar transmitters, because it reduces the number of devices needed to generate sufficient RF power for these applications. Fewer transistors capable of operating at higher temperatures reduces matching and cooling requirements, leading to reduced overall size and cost of these systems. While excellent for fixed-base high-power RF transmission systems, SiC RF transistors are not well suited for portable handheld RF transceivers where drain voltage and power are restricted to function within the operational limitations of small-sized battery packs.

Because rapid progress is being made toward improving the capabilities of SiC RF power transistors, the reader should consult the latest electron device literature for up-to-date SiC RF transistor capabilities. A late-1997 summary of solid-state high-power RF amplification transistor results, including 4H-SiC, 6H-SiC, silicon, GaAs, and GaN device results, is given in Fig. 6.7.[7] Despite the fact that SiC RF transistors are not nearly as optimized, they have still demonstrated higher power densities than silicon and GaAs RF power transistors. The commercial availability of semi-insulating SiC substrates to minimize parasitic capacitances is crucial to the high-frequency performance of SiC RF MESFETs. MESFET devices fabricated on semi-insulating substrates are conceivably less susceptible to adverse yield consequences arising from micropipes than vertical high-power switching devices, primarily because a *c*-axis micropipe can no longer short together two conducting sides of a high field junction in most areas of the lateral channel MESFET structure. In addition to micropipes, other non-idealities, such as variations in epilayer doping and thickness, surface morphological defects, and slow charge trapping/detrapping phenomena causing unwanted device I-V drift,[98] also limit the yield, size, and manufacturability of SiC RF transistors. However, increasingly beneficial SiC RF transistors should continue to evolve as SiC crystal quality and device processing technology continues to improve.

In addition to high-power RF transistors, SiC mixer diodes show excellent promise for reducing undesired intermodulation interference in RF receivers.[99] More than 20-dB dynamic range improvement was demonstrated using non-optimized SiC Schottky diode mixers. Following further development and optimization, SiC-based mixers should improve the interference immunity of a number of RF systems where receivers and high-power transmitters are closely located, as well as improve the reliability and safety of flight RF-based avionics instruments used to guide aircraft in low-visibility weather conditions.

High-Temperature Signal-Level Devices

Most analog signal conditioning and digital logic circuits are considered "signal level" in that individual transistors in these circuits do not require any more than a few milliamperes of current and less than 20 V to function properly. Commercially available silicon-on-insulator circuits can perform complex

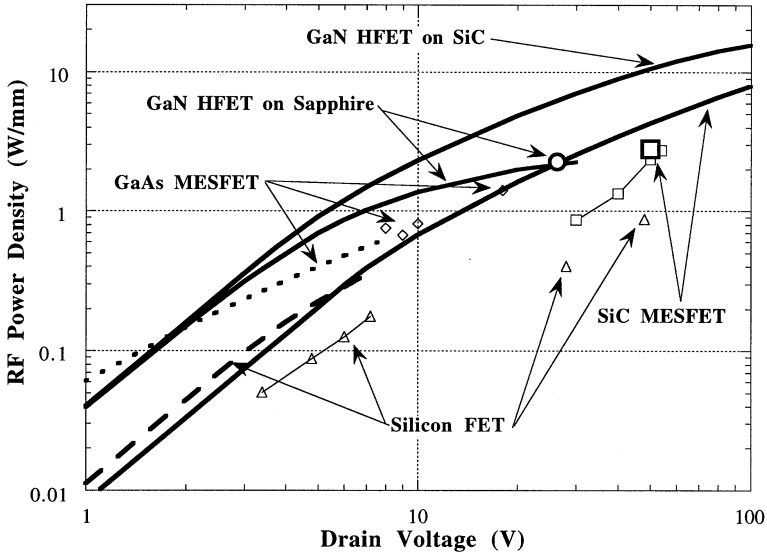

FIGURE 6.7 Theoretical (lines) and experimental (symbols) RF power densities of RF transistors fabricated in silicon, GaAs, SiC, and GaN as of late 1997. (From Ref. 96. With permission.)

digital and analog signal-level functions up to 300°C when high-power output is not required.[100,101] Aside from ICs where it is advantageous to combine signal-level functions with high-power or unique SiC sensors/MEMS onto a single chip, more expensive SiC circuits solely performing low-power signal-level functions appear largely unjustifiable for low-radiation applications at temperatures below 250 to 300°C.

Achieving long-term operational reliability is one of the primary challenges of realizing 300 to 600°C devices and circuits. Circuit technologies that have been used to successfully implement VLSI circuits in silicon and GaAs, such as CMOS, ECL, BiCMOS, DCFL, etc., are to varying degrees candidates for T > 300°C SiC integrated circuits. High temperature gate-insulator reliability (Section 6.5) is critical to the successful realization of MOSFET-based integrated circuits. Gate-to-channel Schottky diode leakage limits the peak operating temperature of SiC MESFET circuits to around 400°C (Section 6.5). Prototype bipolar SiC transistors have exhibited poor gains,[102] but improvements in SiC crystal growth and surface passivation should improve SiC BJT gains.[103] As discussed in Section 6.5, a common obstacle to all technologies is reliable long-term operation of contacts, interconnect, passivation, and packaging at T > 300°C. Because signal-level circuits are operated at relatively low electric fields well below the electrical failure voltage of most micropipes, micropipes affect signal-level circuit process yields to a much lesser degree than they affect high-field power device yields. Non-idealities in SiC epilayers, such as variations in epilayer doping and thickness, surface morphological defects, and slow charge trapping/detrapping phenomena causing unwanted device I–V drift, presently limit the yield, size, and manufacturability of SiC high-temperature integrated circuits.[83] However, continued progress in maturing SiC crystal growth and device fabrication technology should eventually enable the realization of SiC VLSI circuits.

Robust circuit designs that accommodate large changes in device operating parameters with temperature will be necessary for circuits to function successfully over the very wide temperature ranges (as large as 650°C spread) enabled by SiC. While there are similarities to silicon device behavior as a function of temperature, there are also significant differences that will present challenges to SiC integrated circuit designers. For example, in silicon devices, dopant atoms are fully ionized at standard operating temperatures of interest, so that free carrier concentrations correspond with dopant impurity concentrations.[14,15] Therefore, the resistivity of silicon increases with increasing temperature as phonon scattering reduces carrier mobility. SiC device layers, on the other hand, are significantly "frozen-out" due to deeper donor and acceptor dopant ionization energies, so that non-trivial percentages of dopants are not ionized to produce free carriers that carry current at or near room temperature. Thus, the resistivity of SiC layers

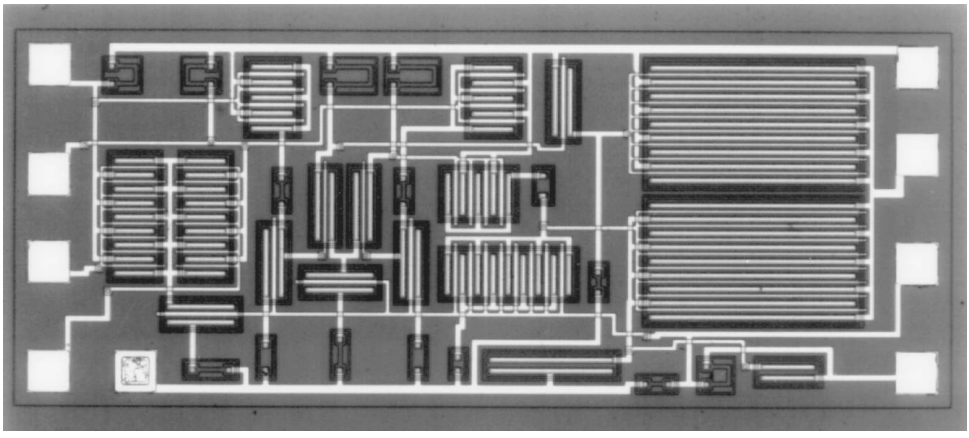

FIGURE 6.8 Optical micrograph of 1 × 2 mm² 300°C 6H-SiC operational amplifier integrated circuit. The chip contains 14 depletion-mode N-channel MOSFETs integrated with 19 resistors. (From Ref. 105. With permission.)

can sometimes initially decrease with increasing temperature as dopant atoms ionize to contribute more current-conducting free carriers, then decrease similar to silicon after most dopant atoms have ionized and increased phonon scattering degrades free carrier mobility. Thus, SiC transistor parameters can exhibit temperature variations not found in silicon devices, so that new device-behavior models are sometimes necessary to carry out proper design of wider-temperature range SiC integrated circuits. Because of carrier freeze-out effects, it will be difficult to realize SiC-based ICs operational at temperatures much lower than –55°C (the lower end of the U.S. Mil-Spec. temperature range).

Small-scale prototype logic and analog amplifier SiC-based ICs (one of which is shown in Fig. 6.8) have been demonstrated using SiC variations of NMOS, CMOS, JFET, and MESFET device topologies.[33,83,104–108] These prototypes are not commercially viable as of this writing, largely due to their high cost, unproven reliability, and limited temperature range that is mostly covered by silicon-on-insulator-based circuitry. However, increasingly capable and economical SiC integrated circuits will continue to evolve as SiC crystal growth and device fabrication technology continues to improve.

SiC High-Power Switching Devices

Operational Limitations Imposed by SiC Material Quality

As discussed in Section 6.3, the most lucrative system benefits of SiC electronics arguably lie in high-power devices. Unfortunately, these devices are also the most susceptible to present-day deficiencies in SiC material quality and process variations, mostly because they operate at high electric fields and high current densities that place the greatest electrical stresses on the semiconductor and surrounding device materials. Prototype SiC devices have demonstrated excellent area-normalized performance, often well beyond (>10X) the theoretical power density of silicon power electronics (Fig. 6.9). However, the presence of micropipe crystal defects has thus far prevented scale-up of small-area prototypes to large areas that can reliably deliver high total operating currents in large-scale power systems, as discussed in Section 6.4 and Refs. 9 and 40. Rectifying power device junctions responsible for OFF-state blocking fail at micropipe defects, leading to undesired (often damaging) localized current flow through micropipes at unacceptably low electric fields well below the critical reverse-breakdown field of defect-free SiC. Over the last decade, SiC micropipe densities have dropped from several hundred per square centimeter of wafer area to tens per square centimeter of wafer area (Section 6.4, Table 6.2), resulting in corresponding improvements in peak SiC device operating currents from less than 1 A to 10s of A. However, further defect reductions of at least an additional order of magnitude will be necessary before reasonably good power device yields and currents will be obtained.

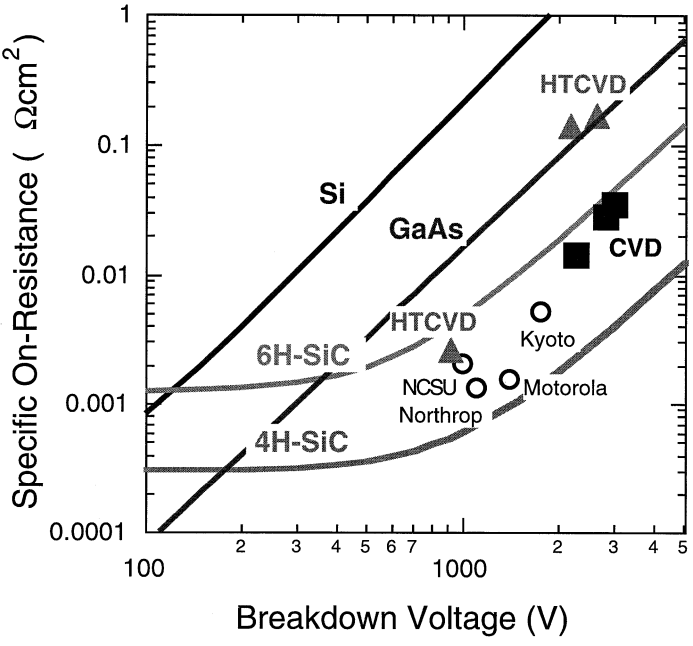

FIGURE 6.9 Experimental SiC (symbols) and theoretical SiC and silicon (lines) Schottky diode specific on resistance plotted as a function of off-state blocking voltage. While the graph clearly shows that the area-normalized performance of small-area SiC devices is orders of magnitude better than silicon, these results have not been successfully upscaled to realize large-area high-current SiC devices due to high densities of device-degrading defects present in commercial SiC wafers and epilayers. (From Ref. 117. With permission.)

In addition to micropipe defects, the density of non-hollow core (elementary) screw dislocation defects in SiC wafers and epilayers has been measured on the order of several thousands per square centimeter of wafer area (Section 6.4). While these defects are not nearly as detrimental to device performance as micropipes, recent experiments have shown that they degrade the leakage and breakdown characteristics of pn junctions.[109,110] Less direct experimental evidence exists to suggest that elementary screw dislocations may also cause localized reductions in minority carrier diffusion lengths[111,112] and non-uniformities and catastrophic localized failure to high-voltage Schottky rectifiers under reverse bias.[72,113] While localized breakdown is well known to adversely degrade silicon device reliability in high-power switching applications, the exact impact of localized breakdown in SiC devices has yet to be quantified. If it turns out that SiC power devices roughly adhere to the same reliability physics well known for silicon power devices, it is possible that SiC devices containing non-hollow core screw dislocations could prove unacceptably unreliable for use in the most demanding high-power conversion applications, such as large-motor control and public power distribution. Thus, these applications might require much larger (i.e., much longer-term) improvements in SiC material quality so as to eliminate all screw dislocations (both hollow core and non-hollow core) from any given device.

SiC High-Voltage Edge Termination

For SiC power devices to successfully function at high voltages, peripheral breakdown due to edge-related electric field crowding[15,16,63] must be avoided through careful device design and proper choice of insulating/passivating dielectric materials. The peak voltage of most prototype high-voltage SiC devices has been limited by often destructive edge-related breakdown, especially in SiC devices capable of blocking multiple kilovolts.[114,115] In addition, most testing of multi-kilovolt SiC devices has required the device to be immersed in specialized high-dielectric strength fluids or gas atmospheres to minimize damaging electrical arcing and surface flashover at device peripheries.[114,116,117]

A variety of edge termination methodologies, many of which were originally pioneered in silicon high-voltage devices, have been applied to prototype SiC power devices with varying degrees of success. Some of these approaches include tailored dopant guard rings,[122–124] tailored etches,[118–121] neutral ion implant damage rings,[125,126] metal guard rings,[127] and anode contact-insulator overlap.[128,129] The higher voltages and higher local electric fields of SiC power devices will place larger stresses on packaging and on wafer insulating materials, so it is unclear that traditional materials used to insulate/passivate silicon high-voltage devices will prove sufficient for reliable use in SiC high-voltage devices, especially if those devices are to be operated at high temperatures.

SiC High-Power Rectifiers

The high-power diode rectifier is a critical building block of power conversion circuits. A good review of experimental SiC rectifier results is given in Ref. 67. As discussed in Refs. 8 and 20 to 22, the most important SiC diode rectifier device design tradeoffs roughly parallel well-known silicon rectifier tradeoffs, except for the fact that numbers for current densities, voltages, power densities, and switching speeds are much higher in SiC. SiC's high breakdown field and wide energy bandgap permit operation of SiC metal–semiconductor Schottky diodes at much higher voltages (i.e., kilovolts) and current densities (kA/cm^2) than is practical with silicon-based Schottky diodes. A drawback of the wide bandgap of SiC is that it requires larger forward bias voltages (~1 V) to reach the turn-on "knee" where significant ON-state current begins flowing, and this can lead to an undesirable increase in ON-state power dissipation. However, the benefits of 100X decreased drift region resistance and much faster dynamic switching should greatly overcome SiC ON-state knee voltage disadvantages in most high-power systems. Figure 6.9 summarizes experimental Schottky diode specific on-resistance versus breakdown voltage results published up through 1997.[117] For blocking voltages up to 3 kV, unipolar SiC Schottky rectifiers offer lower turn-on voltages (~1 to 2 V vs. ~3 V) and faster switching speeds (due to no appreciable minority carrier injection/charge storage) than SiC pn junctions.[21,22]

In rectifiers that block over ~3 kV, bipolar minority carrier charge injection (i.e., conductivity modulation) should enable SiC pn diodes to carry higher current densities than unipolar Schottky diodes whose drift regions conduct solely using dopant-atom majority carriers.[20–22] SiC pn junction blocking voltages as high as 5.5 kV have been realized as of this writing,[130] and further blocking voltage improvements are expected as SiC materials growth and processing further improve. Consistent with silicon rectifier experience, SiC pn junction generation-related reverse leakage is usually smaller than thermionic-assisted Schottky diode reverse leakage. While it has not yet been experimentally verified for SiC, silicon power device experience[131] strongly suggests that SiC pn junction rectifiers should offer significantly better reverse breakdown immunity to overvoltage/overcurrent faults that can occur in high-power switching circuits with large inductors than SiC Schottky rectifiers. As with silicon bipolar devices, reproducible localized control of minority carrier lifetime will be essential in optimizing the switching-speed versus ON-state current density performance tradeoffs of SiC bipolar devices for specific applications. SiC minority carrier lifetimes on the order of several microseconds have been obtained in high-quality epilayers,[132] and lifetime reduction via intentional impurity incorporation and introduction of radiation-induced structural defects appears feasible.

Hybrid Schottky/pn rectifier structures first developed in silicon that combine pn junction reverse blocking with low Schottky forward turn-on should prove extremely useful to realizing application-optimized SiC rectifiers.[133,134] Similarly, combinations of dual Schottky metal structures and trench pinch rectifier structures can also be used to optimize SiC rectifier forward turn-on and reverse leakage properties.[135]

SiC High-Power Switching Transistors

Three terminal power switches that use small drive signals to control large voltages and currents are also critical building blocks of high-power conversion circuits. As well summarized in Ref. 21, a variety of prototype three-terminal SiC power switches have been demonstrated in recent years. For the most part,

SiC solid-state switches are based on well-known silicon device topologies, like the thyristor, vertical MOSFETs, IGBT, GTO, etc., that try to maximize power density via vertical current flow using the substrate as one of the device terminals. Because these switches all contain high-field junctions responsible for blocking current flow in the OFF-state, their maximum operating currents are primarily restricted by the material quality deficiencies discussed in Section 6.6. Therefore, while blocking voltages over 2 kV have been demonstrated in low-current devices,[116] experimental SiC power switches have only realized modest current ratings (under 1 A in most devices).

Silicon power MOSFETs and IGBTs are extremely popular in power circuits, largely because their MOS gate drives are well insulated and require little drive signal power, and the devices are "normally off" in that there is no current flow when the gate is unbiased at 0 V. However, as discussed in Section 6.5, the performance and reliability of SiC power device structures with inversion channel MOS field-effect gates (i.e., MOSFETs, IGBTs, etc.) are limited by poor inversion channel mobilities and questionable oxide reliability at high temperatures. Thus, SiC device structures that do not rely on high-quality gate oxides, such as the thyristor, appear more favorable for more immediate realization, despite some non-trivial drawbacks in operational circuit design and switching speed.

Recently, some non-traditional power switch topologies have been proposed to somewhat alleviate SiC oxide and material quality deficiencies while maintaining normally off insulated gate operation. Shenoy et al.[136] and Hara,[137] respectively, have implemented lateral and vertical doped-channel depletion/accumulation mode power SiC MOSFETs that can be completely depleted by built-in potentials at zero gate bias so that they are "normally off." Spitz et al.[116] recently demonstrated high-voltage SiC lateral MOSFETs implemented on semi-insulating substrates. These devices could conceivably reduce the adverse yield consequences of micropipes, because a *c*-axis micropipe can no longer short together two conducting sides of a high-field junction in most regions of the device. With the assistance of lateral surface electric field tailoring techniques, Baliga[138] has suggested that lateral-conduction SiC power devices could deliver better power densities than traditional vertical SiC power device structures. Baliga has also proposed the advantageous high-voltage switching by pairing a high-voltage SiC MESFET or JFET with a lower-voltage silicon power MOSFET.[138]

SiC for Sensors and Microelectromechanical Systems (MEMS)

Silicon carbide's high-temperature capabilities have enabled the realization of catalytic metal–SiC and metal–insulator–SiC (MIS) prototype gas sensor structures with great promise for emissions monitoring applications.[139,140] High-temperature operation of these structures, not possible with silicon, enables rapid detection of changes in hydrogen and hydrocarbon content to sensitivities of parts-per-million in very small-sized sensors that could easily be placed unobtrusively anywhere on an engine. Once they have been more fully developed, these sensors could assist in active combustion control to reduce harmful pollution emissions from automobile and aircraft engines.

Hesketh's chapter on micromachining describes conventional silicon-based microelectromechanical systems (MEMS). While the previous sections in this chapter have centered on the use of SiC for traditional semiconductor electronic devices, SiC is also likely to play a significant role in emerging MEMS applications.[141] In addition to high-temperature electrical operation, SiC has excellent mechanical properties vital to durable operation of microsystems that address some shortcomings of silicon-based MEMS, such as extreme hardness and low friction, reducing mechanical wear-out as well as excellent chemical inertness to corrosive ambients. Unfortunately, the same properties that make SiC more durable than silicon also make SiC more difficult to process into MEMS structures than silicon. Nevertheless, SiC-based pressure sensors, accelerometers, resonators (Fig. 6.10), and other MEMS systems are being developed for use in harsh-environment applications beyond the reach of silicon-based microsystems. The general approaches to fabricating harsh-environment MEMS structures in SiC and prototype SiC-MEMS results obtained to date are discussed in Ref. 141.

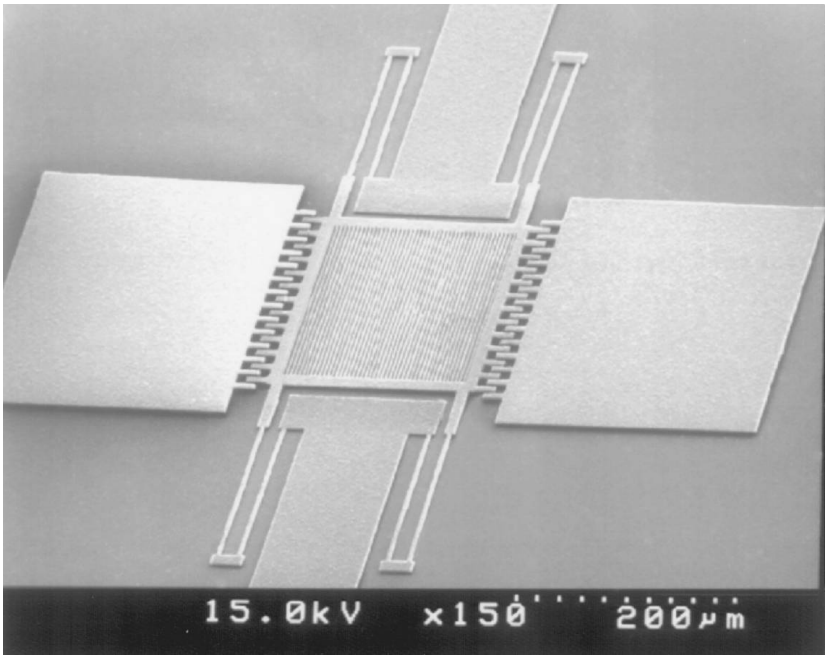

FIGURE 6.10 Micromachined SiC-based lateral resonator device. The excellent mechanical and electrical properties of SiC are enabling the development of harsh-environment microelectromechanical systems (MEMS) for operation beyond the limits of conventional silicon-based MEMS. (From Prof. M. Mehregany, Case Western Reserve University. With permission.)

6.7 Further Recommended Reading

This chapter has presented a brief summary overview of evolving SiC semiconductor device technology. The following publications, which were heavily referenced in this chapter, are highly recommended as advanced, supplemental reading that more completely covers the work being done to develop SiC electronics in much greater technical detail than possible within this short chapter. Reference 12 is a two-volume collection of invited in-depth papers from recognized leaders in SiC technology development that first appeared in special issues of the journal *Physica Status Solidi* (a, 162, No. 1) and (b, 202, No. 1) in 1997. Reference 11 is a two-volume collection of papers from the *7th International Conference on Silicon Carbide, III-Nitrides, and Related Materials* held in Stockholm, Sweden, in September 1997. As SiC electronics is evolving rapidly to fulfill the needs of a steadily increasing array of applications, the reader should consult the current literature for updates on SiC device capabilities. One of the best ongoing sources of SiC electronics information is the *International Conference on Silicon Carbide and Related Materials*, which is held every two years. A meeting was scheduled for October 1999 in Research Triangle Park, North Carolina (internet Web site: www.ISCRM99.ncsu.edu). In addition, a variety of Internet Web sites contain useful SiC information and links, including www.grc.nasa.gov/WWW/SiC/SiC.html, www.hiten.com, www.cree.com, www.ecn.purdue.edu/WBG/, www.sterling-semiconductor.com/, www.imc.kth.se/sic/, and www.ifm.liu.se/Matephys/new_page/research/sic/index.html, among others that can be easily located using widely available World Wide Web Internet search engine services.

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